Amendments to the Drawings:

The attached sheets of drawings include changes to Figures 2, 4, 6, and 8. The sheets, which includes Figures 2, 4, 6, and 8, replace the drawings presented in the previous Amendment dated February 10, 2006. Specifically, Figure 2 is amended to remove solder bumps 215. In addition, Figure 4 is amended to remove solder bumps 415. In addition, Figure 6 is amended to remove solder bumps 615. In addition, Figure 8 is amended to remove solder bumps 815.

A marked-up version of the drawings, with revisions shown in red, is included with the amended drawings. Entry of the amendments to the drawings is respectfully requested.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

The drawings are objected to under 37 CFR 1.83 for reasons stated in the Office Action at page 2, second paragraph. Claims 6, 10 and 16 are cancelled above, therefore removing the feature of the "solder bump" from the claims. Amended Figures 2, 4, 6, and 8 are also attached hereto to replace previously submitted Figures 2, 4, 6, and 8. A marked-up version of Figures 2, 4, 6, and 8 of the drawings, with revisions shown in red, is included with the amended drawings. Reconsideration of the objections to the drawings is respectfully requested.

The amendment filed February 10, 2006 is objected to under 35 U.S.C. 132(a). The Office Action states at page 3 paragraph 1, that the original disclosure discloses that the solder bumps are "not shown" in the drawings, therefore, the drawing structures labeled 215, 415, 615 and 815 cannot be identified as the solder bumps. However, the Applicant respectfully disagrees. While the specification as originally filed recites "not shown", the amendment filed February 10, 2006 amended the specification to remove this language and the drawings were amended to include the feature of the solder bump. The fact that the originally filed specification recites "not shown" does not preclude amending the drawings to show what would be known to one of skill in the art. The solder bumps , 215, 415, 615 and 815 can be added because one of skill in the art based on the specification at least at page 6, lines 29-31, page 7, lines 12-13, page 8, lines 13-14, page 9, lines 24-26, and page 10 lines 7-8 would know that the solder bumps are present and would be located as shown in the amended drawings submitted with the Amendment filed February 10, 2006.

Notwithstanding the above remarks, claims 6, 10 and 16 are cancelled and the specification and drawings are amended herein to remove the material added by the previous Amendment.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Corisis (U.S. Patent Number 6,607,937). Claims 2-4, 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis in view of Bolkin, *et al.* (U.S. Patent Number 6,798,057). Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Bolkin, *et al.* and further in view of Koh, *et al.* (U.S. Patent Number 6,737,738). Claims 6-8 are rejected under 35 U.S.C.

103(a) as being unpatentable over Corisis, Bolkin, *et al.*, and Koh, *et al.* and further in view of Yanagida (U.S. Publication Number 2001/0042923) and Jiang, *et al.* (U.S. Patent Number 6,906,415). Claims 10-12 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-5, 7, 9, 11, 12, 15 and 17, a multi-chip package includes a first semiconductor chip, which shows good results when tested for reliability after assembled at a packaged level. The first semiconductor chip includes a flash memory.

Claims 1-5, 7, 9, 11, 12, 15 and 17 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the first semiconductor chip includes a flash memory. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

With regard to the rejection of claim 1, Corisis discloses, in FIG. 3, a lower packaged device 220a that includes a first microelectronic die 224a mounted to a package substrate 240 and an encapsulating material 223 that encases the microelectronic die 224a. In FIG. 5 of Corisis, a packaged device 420 that includes a microelectronic die 424a mounted to a package substrate 440 and an encapsulating material 423a. A microelectronic die 424b mounted directly to the first encapsulating material 423a.

Corisis fails to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. There is no mention in Corisis of a flash memory being included in the lower packaged device.

Corisis fails to teach or suggest certain elements of the invention set forth in the claims. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claim 1 under 35 U.S.C. 102(e) based on Corisis is respectfully requested.

With regard to the rejection of claims 2-4, 9 and 15 under 35 U.S.C. 103(a) over Corisis in view of Bolkin, *et al.*, Bolkin, *et al.* discloses a first die 102 is an ASIC device and a second die 104 is a flash memory device. Each die 102 and 104 is attached to an interposer 101.

Bolkin, *et al.* fails to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. Instead, in Bolkin, *et al.*, the flash memory device 104 is a die and is therefore not packaged. A first semiconductor of the present invention as claimed is packaged. Further, Corisis discloses a lower packaged device 220a, 420. Therefore, the unpackaged die 104 of Bolkin, *et al.* cannot be combined with Corisis.

Corisis and Bolkin, *et al.* fail to teach or suggest elements of the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Specifically, Corisis and Bolkin, *et al.* fail to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Therefore, it is believed that claims 1-5, 7, 9, 11, 12, 15 and 17 are allowable over the cited references, and reconsideration of the rejections of claims 2-4, 9 and 15 under 35 U.S.C. § 103(a) based on Corisis and Bolkin, *et al.*, is respectfully requested.

With regard to the rejection of claim 5 under 35 U.S.C. 103(a) over Corisis, Bolkin, *et al.* and Koh, *et al.*, Koh, *et al.* discloses a first IC package 22 and a second IC package 24 that are separated from each other by an airspace 23.

Like Corisis and Bolkin, *et al.*, Koh, *et al.* fails to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. There is no mention in Koh, *et al.* of a flash memory being included in the first IC package 22 or the second IC package 24.

Corisis, Bolkin, *et al.* and Koh, *et al.* fail to teach or suggest elements of the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Specifically, Corisis, Bolkin, *et al.* and Koh, *et al.* fail to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Therefore, it is believed that claims 1-5, 7, 9, 11, 12, 15 and 17 are allowable over the cited references, and

reconsideration of the rejections of claim 5 under 35 U.S.C. § 103(a) based on Corisis, Bolkin, *et al.* and Koh, *et al.*, is respectfully requested.

With regard to the rejection of claims 6-8 under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, Koh, *et al.*,Yanagida, and Jiang, *et al.*, it is submitted that Yanagida and Jiang, *et al.*, like Corisis, Bolkin, *et al.*, and Koh, *et al.*, fail to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. There is no mention of a flash memory in either of Yanagida, and Jiang, *et al.*

It is therefore submitted that Corisis, Bolkin, *et al.* and Koh, *et al.* fail to teach or suggest elements of the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Specifically, Corisis, Bolkin, *et al.* and Koh, *et al.* fail to teach or suggest a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Therefore, it is believed that claims 1-5, 7, 9, 11, 12, 15 and 17 are allowable over the cited references, and reconsideration of the rejections of claims 6-8 under 35 U.S.C. § 103(a) based on Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.*, is respectfully requested.

With regard to the rejection of claims 10-12 and 16-18 under 35 U.S.C. 103(a) as being unpatentable over Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.*, it is submitted that none of the Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* references teaches or suggests a multi-chip package that includes a first semiconductor chip that includes a flash memory, as claimed.

It is therefore submitted that Corisis, Bolkin, *et al.*, Yanagida, and Jiang, *et al.* fail to teach or suggest elements of the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-5, 7, 9, 11, 12, 15 and 17. Therefore, it is believed that claims 1-5, 7, 9, 11, 12, 15 and 17 are allowable over the cited references, and reconsideration of the

rejections of claims 10-12 and 16-18 under 35 U.S.C. § 103(a) based on Corisis, Bolkin, *et al.*, Koh, *et al.*, Yanagida, and Jiang, *et al.*, is respectfully requested.

The Office Action indicates at page 17, paragraphs 1-4, that the applicant and assignee of the application are required under 37 C.F.R. 1.105 to provide information to the examiner. In FIGs. 2, 4, 6 and 8, the shaded and unshaded portions of the first semiconductor chip 210, 410, 610 and 810 are combined to form the first semiconductor chip 210, 410, 610 and 810, respectively. The shaded portions of the first semiconductor chip 210, 410, 610 and 810 are protective coverings and the unshaded portions of the first semiconductor chips 210, 410, 610 and 810 are the semiconductor die. This would be obvious to one of skill in the art based on the specification at least at page 5, lines 15-22, and page 6, lines 17-24. In contrast, the second and third semiconductor chips are good die (bare chip) (see the specification at page 5, lines 23-24 and page 6, lines 3-4). The shaded portion being a protective covering and the unshaded portion being a semiconductor die would be obvious to one of skill in the art. For example, in FIG. 3 of Corisis, a lower packaged device 22a includes a first microelectronic die 224a and an encapsulating material 223 that encases the microelectronic die 224a.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 7/24/06

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FIG. 2

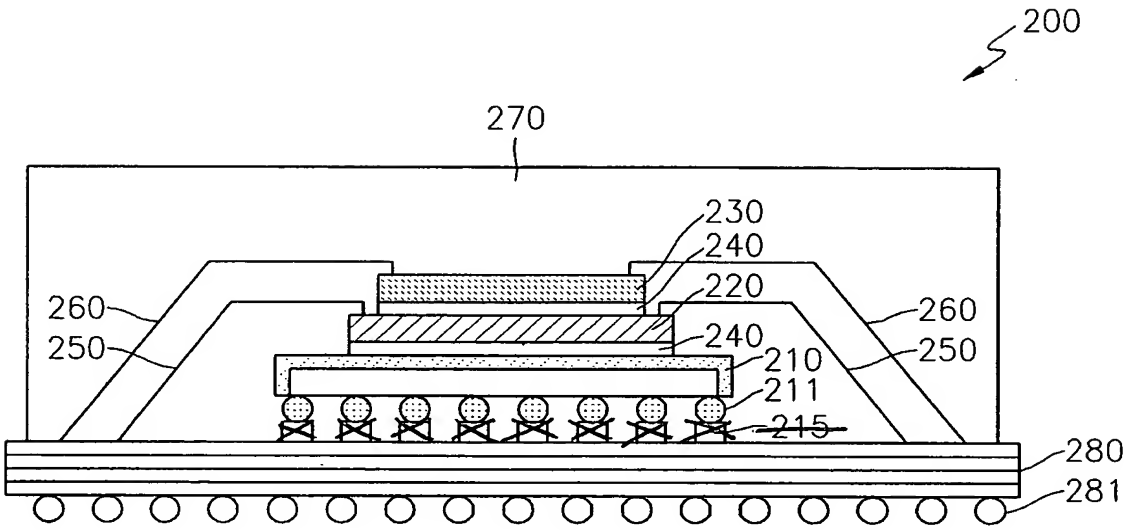
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FIG. 3

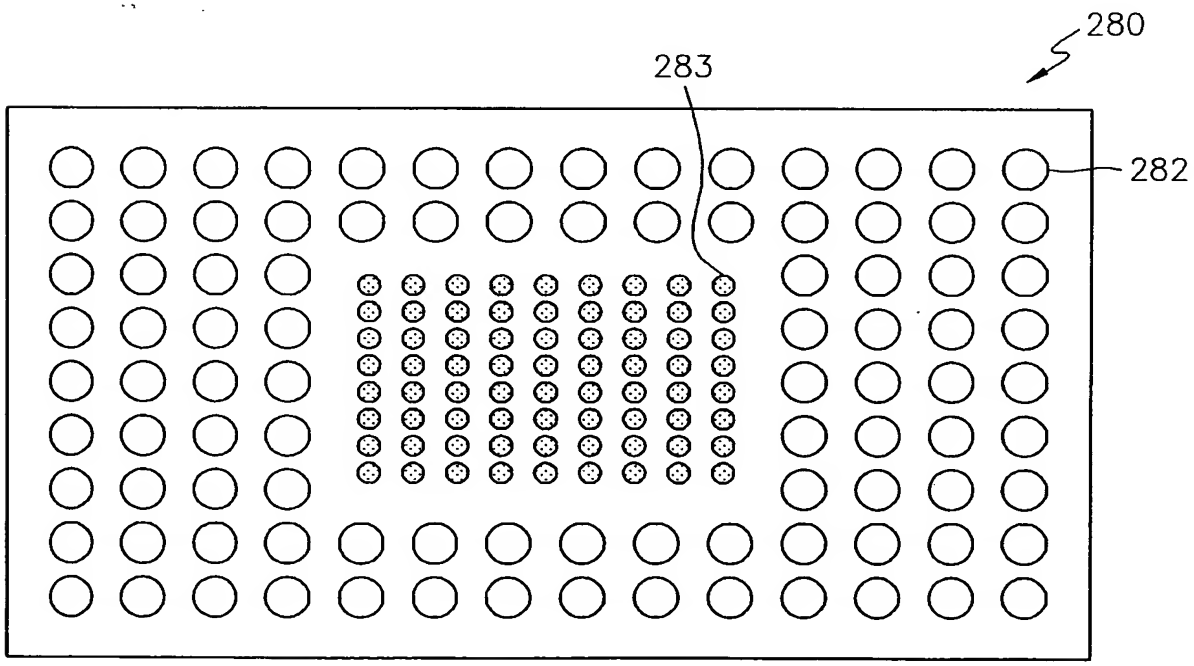
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FIG. 4

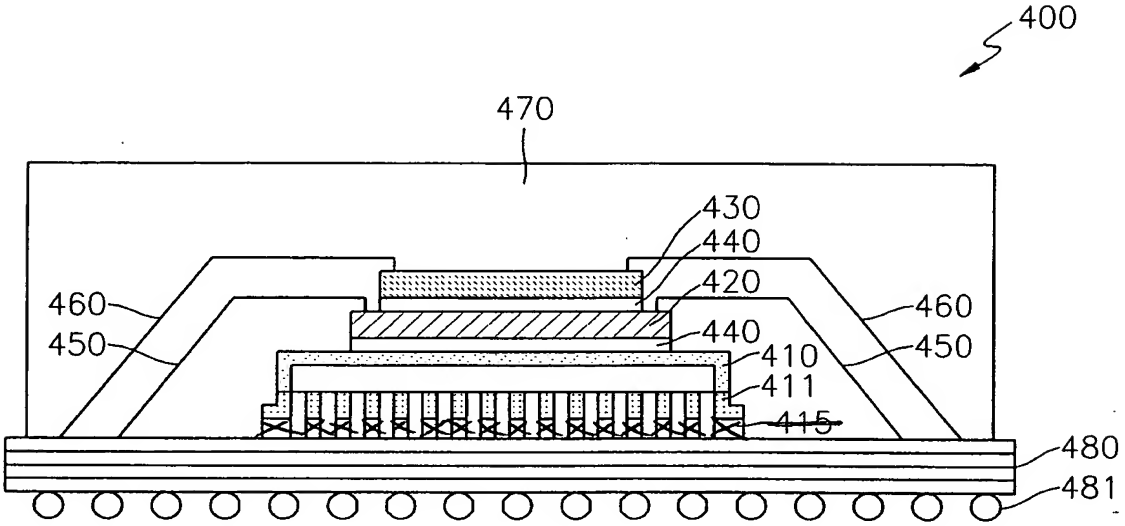
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FIG. 5

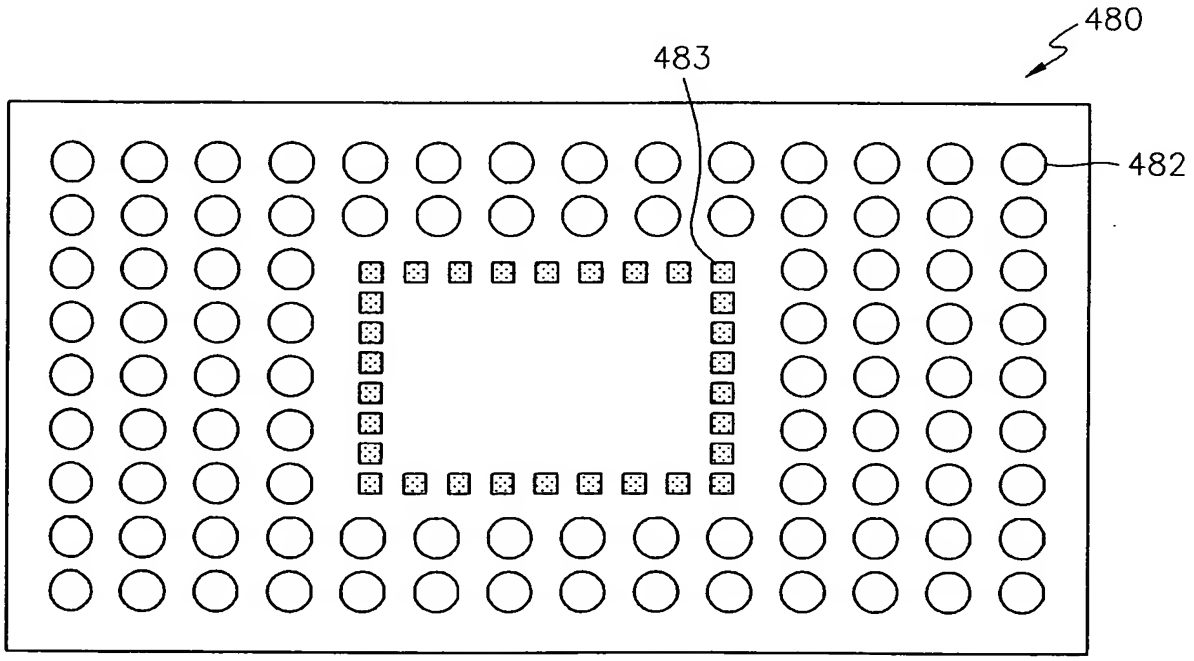
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FIG. 6

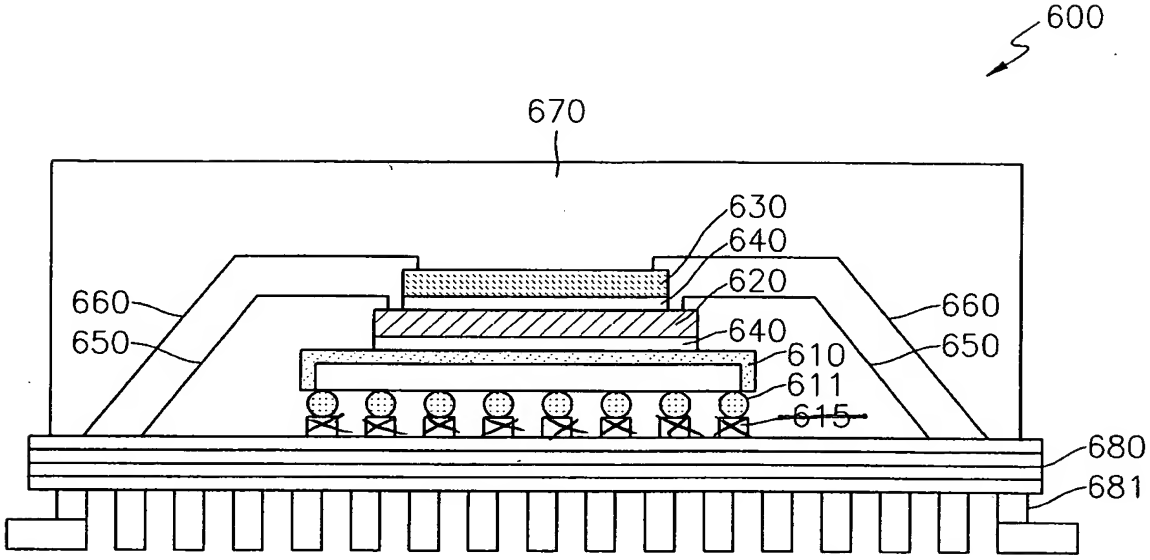
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FIG. 7

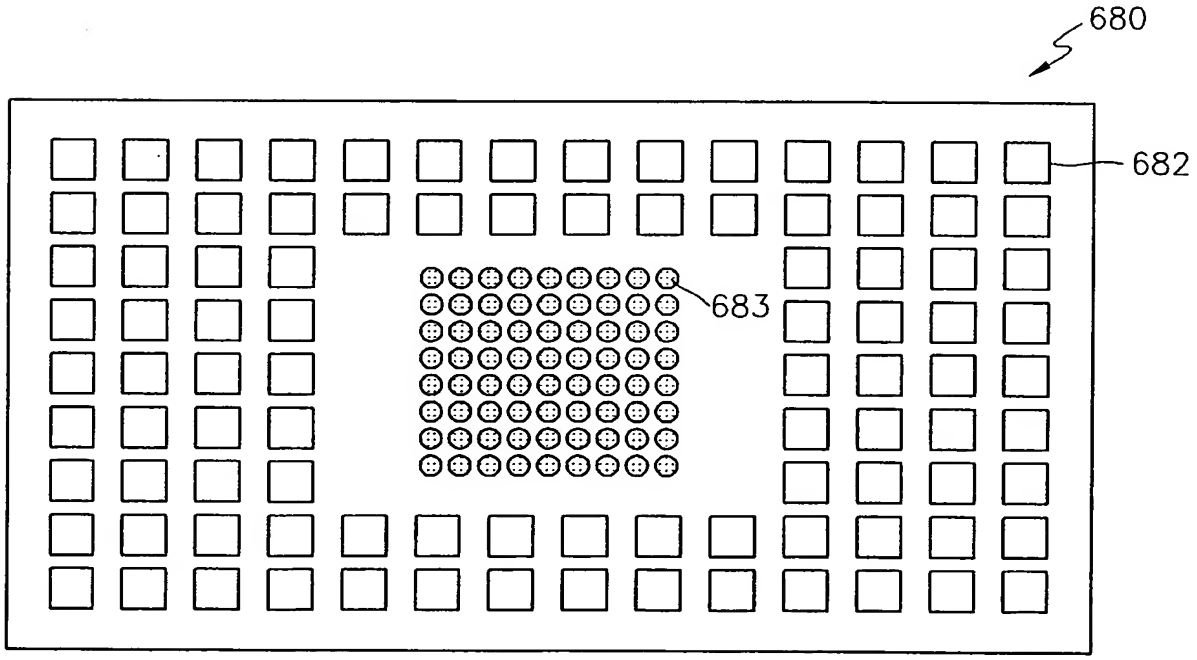
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FIG. 8

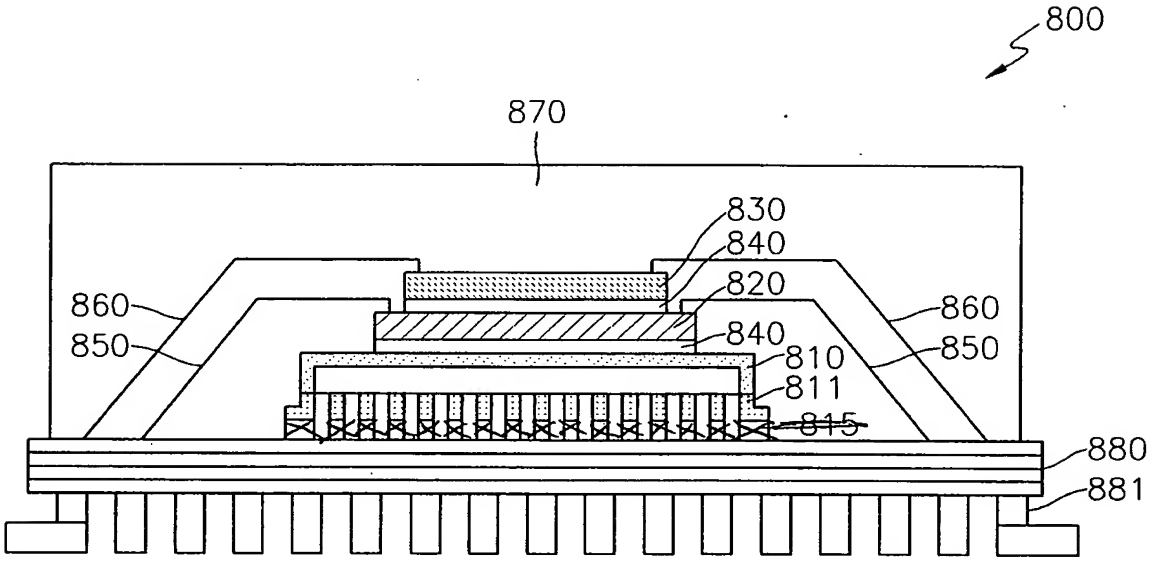
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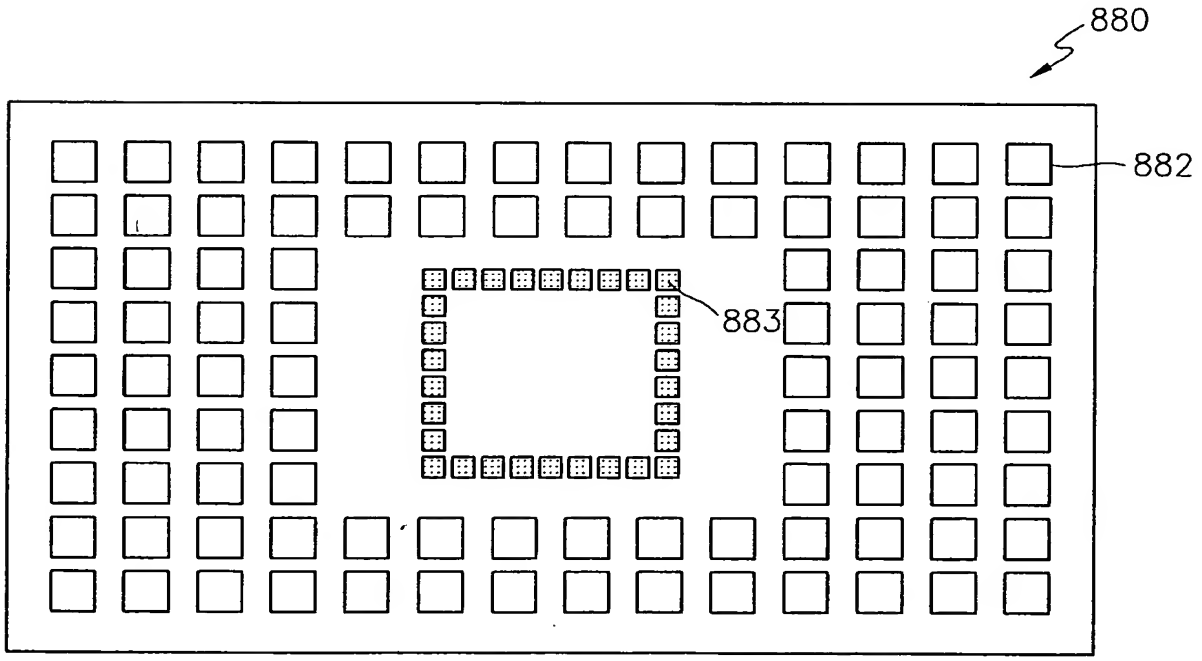
FIG. 9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